AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-4. (Canceled without prejudice or disclaimer).

5. (Currently Amended) A semiconductor integrated circuit device comprising:

~~a first CPU accessing a first memory space with address translations and a second memory space without address translations;~~

a CPU related to a first memory space;

a peripheral LSI related to a second memory space;

a CPU bus connected between the CPU and the peripheral LSI and related to the first memory space; and

an I/O bus connected to the peripheral LSI and related to the second memory space;

wherein the peripheral LSI comprises:

an address translation circuit;

a nonvolatile memory to store address information indicating a relationship between an address of the first memory space and an address of the second memory space; and

a CODEC circuit to compress and uncompress video data;

a first protocol decode and generation circuit connecting to a first bus connected to the first memory space; and

a second protocol decode and generation circuit connecting to a second bus connected to the second memory space;

wherein the address translation circuit is connected to the first and second protocol decode and generation circuits and comprises:

a register, and

an address calculation circuit,

wherein, when the semiconductor integrated circuit is initialized, the register reads the address information from the nonvolatile memory; ~~and~~

wherein, when the CPU acts as a bus master to access the second memory space, the first protocol decode and generation circuit receives a first address in the first memory space and sends the first address to the address calculation circuit, the address calculation circuit translates the first address into a second address in the second memory space from the address information stored in the register, and the address calculation circuit sends the second address to the first protocol decode and generation circuit;

wherein, when the ~~semiconductor integrated circuit~~ peripheral LSI acts as a bus master to access the first memory space, the second protocol decode and generation circuit receives a ~~first~~ third address in the second memory space and sends the ~~first~~ third address to the address calculation circuit, the address calculation circuit translates the ~~first~~ third address into a ~~second~~ fourth address in the first memory space from the address information stored in the register, and the

address calculation circuit sends the ~~second~~ fourth address to the first protocol decode and generation circuit; and

wherein the uncompressed video data is transferred through the peripheral LSI from the CPU bus to the I/O bus after the CODEC circuit uncompresses the compressed video data; and

wherein the compressed video data is transferred through the peripheral LSI from the I/O bus to the CPU bus after the CODEC circuit compresses the video data.

6. (Previously Presented) The semiconductor integrated circuit according to claim 5, wherein the address information is stored in the nonvolatile memory when a probing test is conducted on the semiconductor integrated circuit.

7. (Currently Amended) A semiconductor integrated circuit device comprising:

a CPU related to a first memory space;

a peripheral LSI related to a second memory space;

a CPU bus connected between the CPU and the peripheral LSI and related to the first memory space; and

an I/O bus connected to the peripheral LSI and related to the second memory space;

wherein the peripheral LSI comprises:

~~a first CPU accessing a first memory space with address translations and a second memory space without address translations;~~

an address translation circuit;

a nonvolatile memory; and

a CODEC circuit to compress and uncompress video data;

a first protocol decode and generation circuit connecting to a first bus connected to the first memory space; and

a second protocol decode and generation circuit connecting to a second bus connected to the second memory space;

wherein the address translation circuit is connected to the first and second protocol decode and generation circuits and comprises:

a register, and

an address calculation circuit,

wherein the nonvolatile memory stores a first start address in a first memory range belonging to the first memory space and a second start address in a second memory range belong to the second memory space;

wherein the second memory range is allocated to the first memory range;

wherein, when the semiconductor integrated circuit is initialized, the register reads the first start address and the second start address from the nonvolatile memory; ~~and~~

wherein, when the CPU acts as a bus master to access the second memory space, the first protocol decode and generation circuit receives a first address in the first memory space and sends the first address to the address calculation circuit, the address calculation circuit translates the first address into a second address in the second memory space from the address information stored in the register, and the address calculation circuit sends the second address to the first protocol decode and generation circuit;

wherein, when ~~semiconductor integrated circuit~~ the peripheral LSI acts as a bus master to access the first memory space, the second protocol decode and generation circuit receives a ~~first~~ third address in the second memory range and sends the ~~first~~ third address to the address calculation circuit, the address calculation circuit translates the ~~first~~ third address into a ~~second~~ fourth address in the first memory range from the first start memory address, the second start memory address, and the ~~first~~ third address which are stored in the register, and the address calculation circuit sends the ~~second~~ fourth address to the first protocol decode and generation circuit, and

wherein the uncompressed video data is transferred through the peripheral LSI from the CPU bus to the I/O bus after the CODEC circuit uncompresses the compressed video data; and

wherein the compressed video data is transferred through the peripheral LSI from the I/O bus to the CPU bus after the CODEC circuit compresses the video data.

8. (Currently Amended) The semiconductor integrated circuit according to claim 7:

wherein the address calculation circuit translates the ~~first~~ third address into the ~~second~~ fourth address from a formula: the first start address + the ~~first~~ third address - the second start address.

9. (Currently Amended) The semiconductor integrated circuit according to claim 7:

wherein the nonvolatile memory further stores a first address width of the first memory range;

wherein the address translation circuit further comprises an address selection circuit and an interrupt circuit;

wherein, when the semiconductor integrated circuit acts as a bus master to access the first memory space, the address selection circuit decides whether or not the first address belongs to the second memory range; and

wherein the address selection circuit ~~sends~~ outputs an error signal ~~to the address selection circuit~~ if the first address doesn't belong to the second memory range.

10. (Currently Amended) The semiconductor integrated circuit according to claim 7:

wherein the nonvolatile memory stores a third start address in a third memory range belonging to the second memory space and a fourth start address in a fourth memory ~~address~~ range belonging to the first memory space;

wherein the fourth memory range is allocated to the third memory range;

wherein, when the semiconductor integrated circuit is initialized, the register reads the third start address and the fourth start address from the nonvolatile memory; and

wherein, when a second CPU acts as a bus master to access the second memory space, the first protocol decode and generation circuit receives a ~~third~~ fifth address in the first memory range and sends the ~~third~~ fifth address to the address calculation circuit, the address calculation circuit translates the ~~third~~ fifth address into

a ~~fourth~~ sixth address in the fourth memory range from the third start memory address, the fourth start address, and the ~~third~~ fifth address which are stored in the register, and the address calculation circuit sends the ~~fourth~~ sixth address to the second protocol decode and generation circuit.

11. (Previously Presented) A semiconductor integrated circuit according to claim 5, wherein the address translation circuit is part of a flexible bus controller which is separate from the CPU.

12. (Previously Presented) A semiconductor integrated circuit according to claim 7, wherein the address translation circuit is part of a flexible bus controller which is separate from the CPU.

13. (Previously Presented) A semiconductor integrated circuit according to claim 11, wherein said flexible bus controller further comprises said first and second protocol decode and generation circuits.

14. (Previously Presented) A semiconductor integrated circuit according to claim 12, wherein said flexible bus controller further comprises said first and second protocol decode and generation circuits.

15. (Currently Amended) A semiconductor integrated circuit comprising:

a CPU related to a first memory space;

a peripheral LSI related to a second memory space;

a CPU bus connected between the CPU and the peripheral LSI and related to the first memory space; and

an I/O bus connected to the peripheral LSI and related to the second memory space;

~~a first CPU accessing a first memory space with address translations and the second memory space without address translations;~~

wherein the ~~a~~ peripheral LSI, is separate from the first CPU, and is adapted to transfer data between said first CPU and a peripheral device, said peripheral LSI comprising:

an address translation circuit;

a nonvolatile memory to store address information indicating a relationship between an address of the first memory space and an address of the second memory space;

a CODEC circuit to compress and uncompress video data;

a first protocol decode and generation circuit connecting to a first bus connected to the first memory space; and

a second protocol decode and generation circuit connecting to a second bus connected to the second memory space;

wherein the address translation circuit is connected to the first and second protocol decode and generation circuits and comprises:

a register, and

an address calculation circuit,

wherein, when the CPU acts as a bus master to access the second memory space, the first protocol decode and generation circuit receives a first address in the first memory space and sends the first address to the address calculation circuit, the address calculation circuit translates the first address into a second address in the second memory space from the address information stored in the register, and the address calculation circuit sends the second address to the first protocol decode and generation circuit;

wherein the uncompressed video data is transferred through the peripheral LSI from the CPU bus to the I/O bus after the CODEC circuit uncompresses the compressed video data; and

wherein the compressed video data is transferred through the peripheral LSI from the I/O bus to the CPU bus after the CODEC circuit compresses the video data.

16. (Previously Presented) A semiconductor integrated circuit according to claim 15, wherein the peripheral LSI further comprised a flexible bus controller which includes said address translation circuit and said first and second protocol decode and generation circuits.

17. (New) The semiconductor integrated circuit device according to claim 5, further comprising:

a first memory;

a second memory;

a flash memory; and

an LCD controller;

wherein the first memory and the flash memory are connected to the CPU bus; and

wherein the second memory and the LCD controller are connected to a camera.

18. (New) The semiconductor integrated circuit device according to claim 7, further comprising:

a first memory;

a second memory;

a flash memory; and

an LCD controller;

wherein the first memory and the flash memory are connected to the CPU bus; and

wherein the second memory and the LCD controller are connected to a camera.

19. (New) The semiconductor integrated circuit device according to claim 15, further comprising:

a first memory;

a second memory;

a flash memory; and

an LCD controller;

wherein the first memory and the flash memory are connected to the CPU bus; and

wherein the second memory and the LCD controller are connected to a camera.